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A T-Type Modular Multilevel Converter

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***Abstract*- This paper proposes a novel modular multilevel converter (MMC) named 'T-type MMC' (T-MMC) for reliable, controllable and efficient performance in energy conversion applications. Circuitry configurations and control structures are presented, with respect to fundamental and additional functions. The T-MMC topology consists of two solid-state power stages (Stage-I and Stage-II), which are coordinated for ac and dc fault tolerance, increased ac-side voltage synthesis, etc. Energy storage elements can be integrated into the submodules. As a result, the T-MMC based energy storage system can not only increase system inertia but maintain continuous power transmission during faults. A thyristor forced-commutation technique facilitates actively-controlled utilization of symmetrical thyristors in the conduction path; thus T-MMC normal-mode operation losses can be equivalent to those of the conventional half-bridge MMC. Simulation and experimentation demonstrate the performance of the T-MMC.**

Index Terms − T-Type Modular Multilevel Converter, ac/dc fault, thyristor, energy storage system.

I. Introduction

The electric power world is undergoing unprecedented evolution, where generation, transmission and distribution need advanced systems and converters of higher sustainability, operability and security. Stable and efficient power converters are demanded, especially for bulk power applications such as the medium to high voltage direct current (MVDC/HVDC) systems, medium-voltage motor drives, and flexible ac transmission systems (FACTS) [1]-[4]. Based on the concept of power building block (PBB) strings for scalability and modularity, modular multilevel converters (MMCs) exhibit advantageous features and have been widely implemented [2].

Various voltage source converters (VSCs) that use different submodules (SMs) as the PBB have been investigated to gain merits such as dc fault ride-through capability and higher efficiency. In general, unipolar or bipolar voltage generation ability of SMs (half-bridge HB and full-bridge FB are representatives) determines the dc fault blocking competency of a converter [3], [4]. However, SMs with the reverse-voltage blocking ability increase the number of switches in the main conduction path, impairing the high-efficiency feature of the overall converter. As a result, any design has to evaluate its constructed PBBs and the trade-off between a larger arm operational range (indicating dc fault resilience) and the lower semiconductor losses [5], [6]. Consequently, mixed-cell MMC types based on the combination of conventional HB and other SMs (such as FBs or degraded FBs) have attracted attention as they balance efficiency and dc fault tolerance capability [7]-[9]. The alternate arm converter based on director switches and FB SMs has a compact size and dc fault isolation capability, but smooth waveform synthesis is difficult and arm operational range is limited [10]. An MMC based on unidirectional current FB SMs is proposed with much lower IGBT usage and dc fault blocking capability; however, specific control systems and application scenarios are needed [11].

Another MMC construction deploys series-connected PBBs in the ac side. These topologies, with a specific harmonic elimination modulation, were proposed to optimize the conventional two-level converter in terms of ac output quality, switching losses, and dc fault blocking ability [12]-[14]. Three-phase series and parallel hybrid MMCs were later proposed based on the same director-switch concept [15]. However, the high *dv*/*dt* stress over director switches is the main problem for high voltage applications, and although the series-connected configuration distributes the dc-link voltage into three levels, balancing capacitor voltages needs intricate control, especially during unbalanced grid faults. Then, topologies with sufficient FB SMs were proposed in [16] and [17] to gain dc fault ride-through capability in HVDC applications, and the MMC behaves as a two-level converter using a quasi two-level modulation technique [18]. Aimed at connecting large wind turbines into the grid with the high-quality ac output, a hybrid MMC combines an HB MMC with an FB SM, as proposed in [19]. However, ac-side FB links of such designs are always in operation; thus, the mentioned trade-off is not overcome.

Attracted by the salient conducting feature of thyristors, researchers have integrated thyristor-based switches into the VSCs. Four hybrid topologies combining SMs with line-commutated converters (LCCs) were reviewed in terms of active and reactive power capabilities [20]. With the design concept inherited from LCCs, various VSC configurations based on FB SMs and thyristor strings have been investigated [21]-[24]. However, different from the conventional LCC implementation, the series-connection of thyristors requires

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higher-performance voltage-balancing and signal-synchronizing techniques for forced-commutation approaches, and sophisticated turn-on/off processes occur at the fundamental frequency, which may result in voltage-balancing or commutation failure. A novel dc-fault tolerant MMC was proposed, with fully-controllable thyristors (IGCTs or GTOs) adopted for switching action [25]. Thus, the major issue is that thyristor high voltage and current capabilities are not fully utilized.

Power system inertia is reducing globally as the penetration of converter-interfaced generation decreases intrinsic energy storage ability [26]. Issues of intermittent energy sources tend to threaten the normal operation of power systems as well. Also, pulse power consumption and system faults in either the dc or ac grid may induce sudden power variations. Thus, smoothing the power transmission in contingencies is required to maintain safe and stable system operation. Integrating energy storage systems (ESSs) into the power system, in short, medium and long terms, becomes urgent for the sake of security and management [27]. However, both energy storage technologies and ESS integration approaches have technical limitations and practical challenges in medium and high voltage applications, which impede their exploitation [28], [29]. Integrating batteries or supercapacitors into the MMC is a promising approach as such energy storage elements (ESEs) are suitable for distributed utilization and the converter can perform as a battery/supercapacitor management system [30]-[33]. Associated control systems and behavior of ESE-equipped MMCs are presented [34]-[37]. Although the value of decoupling ac and dc side powers is observed, such MMC-based ESS is rarely investigated in system fault scenarios, where maintaining continuous power transfer is required for the system security. One reason is that the power exchanging capability of conventional ESS is impaired when the parallel-connected network has a fault. By integrating batteries into the mixed-cell MMC for a medium voltage shipboard power system, continuous power flow is enabled during both ac and dc faults [38]. But the battery transient current rating is limited in high power applications, and the normal-mode operation efficiency is similar to that reported in [7].

In light of this discussion, this paper proposes a T-type MMC (T-MMC) based on a dual-stage structure which offers benefits such as ac-side voltage enlargement and dc/ac fault ride-through. Additionally, due to the deployment of thyristors, operation losses of Stage-II under normal conditions are significantly reduced, leading to the overall converter being as efficient as the conventional HB MMC. After integrating ESEs, the T-MMC can perform as a flexible ESS, enabling regular energy storage, advanced grid ancillary services provision and dc/active power support during system intermittency and faults. As a result, the security, stability and reliability of interconnected dc and ac systems are greatly enhanced. Functions and performances are elaborated in this paper, with simulation and experimental verification.

The remainder of the paper is organized as follows. Sections II describes the structure and basic characteristics of the proposed T-MMC, whereas Section III discusses the thyristor-commutation approach. The T-MMC based ESS and its additional features are presented in Section IV. Section V presents the control strategy. Simulation evaluation and experimentation results are provided in sections VI and VII,

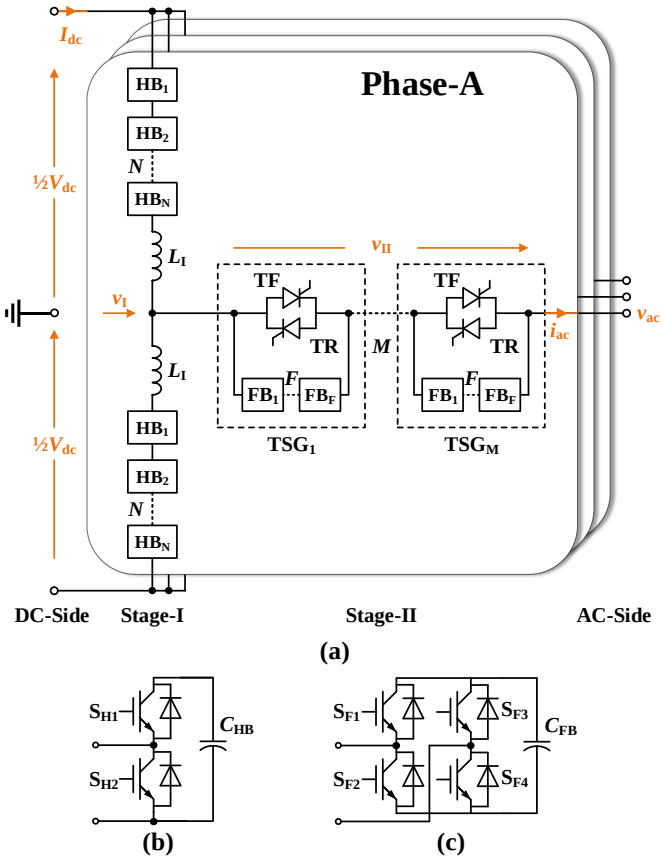

Fig. 1. The T-MMC circuit configurations. (a) Topology diagram. (b) HB SM. (c) FB SM.

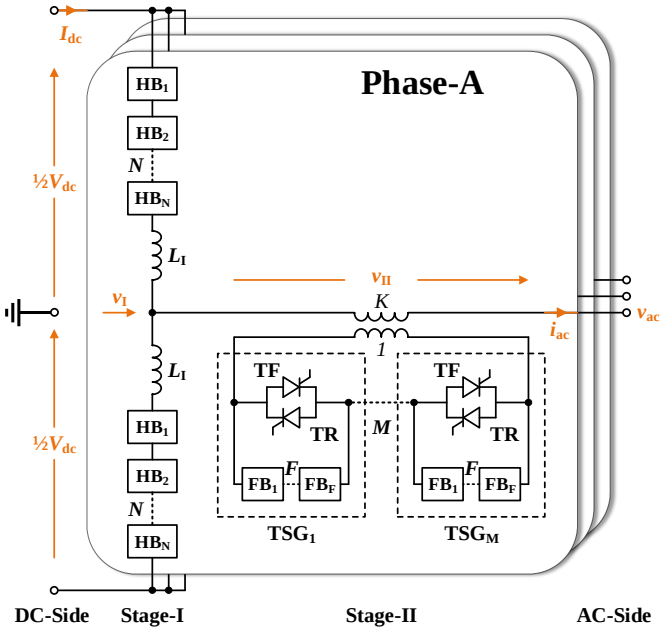

Fig. 2. The T-MMC topology with series-connected isolation transformer.

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respectively, to validate technical feasibility and critical functions. Finally, Section VIII concludes this study.

II. Topologies and Fundamental Functions of the Proposed T-Type Modular Multilevel Converter

Fig. 1 shows the basic topology, and constructed HB and FB SMs of the proposed T-MMC. One T-MMC phase consists of three star-connected modular arms, with their ends as dc positive, dc negative and ac nodes respectively, resembling the letter 'T'. The dc-side power interface (Stage-I) has upper and lower arms, where each consists of N HB SMs and an arm inductor (L_I) as that of a conventional HB MMC, whereas the ac-side power interface (Stage-II) is one arm composed of M thyristor-SM groups (TSGs). As shown in Fig. 1, within one TSG, a pair of antiparallel-connected symmetric (reverse blocking) thyristors (TF//TRs) and F series-connected FB SMs form two parallel current paths, both of which are designed for bidirectional current flow. Auxiliary circuits such as the snubbers and any protective SM parallel-connected thyristors are not illustrated for simplicity.

From the topology feature perspective, the proposed T-MMC is a VSC with modularity and scalability. Within each stage, equal voltage distribution can be achieved between IGBTs and thyristors respectively, as long as HB and FB SM capacitor voltages are maintained balanced. The shunt TF//TRs of Stage-II are on during normal operation; thus, taking advantage of thyristor features (high voltage and power capabilities), minimal voltage drop and low conduction loss are incurred by Stage-II. The proposed TSG can also ensure successful thyristor-commutation, which will be presented later. Like a conventional HB MMC, the HB SM voltage rating of Stage-I is V_{dc}/N, and Stage-I can synthesize a sinusoidal voltage $v_I = V_I \sin(\omega t+\varphi_I)$. Assuming all Stage-II TF//TRs are off, and FB SM capacitor voltages are equal and constant, Stage-II is able to synthesize a sinusoidal voltage $v_{II} = V_{II} \sin(\omega t+\varphi_{II})$. Then the voltage ratings of the TF//TRs and the FB SMs, namely, V_T and V_{FB}, are V_{II}/M and $V_{II}/(M\times F)$, respectively. Without loss of generality, V_I equals V_{II}, for fulfilling all functions of the proposed T-MMC.

A galvanic isolated topology variant is shown in Fig. 2, where the TSG voltage level can also be flexibly changed by the transformer turning ratio K. Accordingly, V_T and V_{FB} are $V_{II}/(M\times K)$ and $V_{II}/(M\times F\times K)$, respectively. The transformer bandwidth must be commensurate with the highest frequency of required compensating harmonics.

This MMC type can be applied in various power system and motor drive scenarios. In generic grid-connected applications, the T-MMC ac-side terminal is connected to the ac grid point of common coupling (PCC) through a grid-interfacing transformer, as shown in Fig. 3(a), where the T-MMC is employed as a bidirectional dc/ac converter station. Thus the T-MMC can be modeled as the series-connected ac voltage sources, as shown for one phase in Fig. 3(b), where L and R represent the ac bus impedance. Different operational modes can be achieved by manipulating the two stages. Fig. 4 illustrates four fundamental modes (modes 1 to 4) of the proposed T-MMC (one phase) under network normal and faulty conditions.

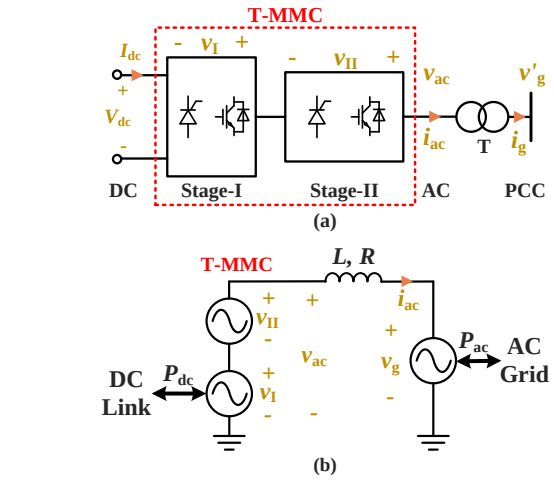

Fig. 3. T-MMC in grid-connected applications. (a) Schematics. (b) Analytical model.

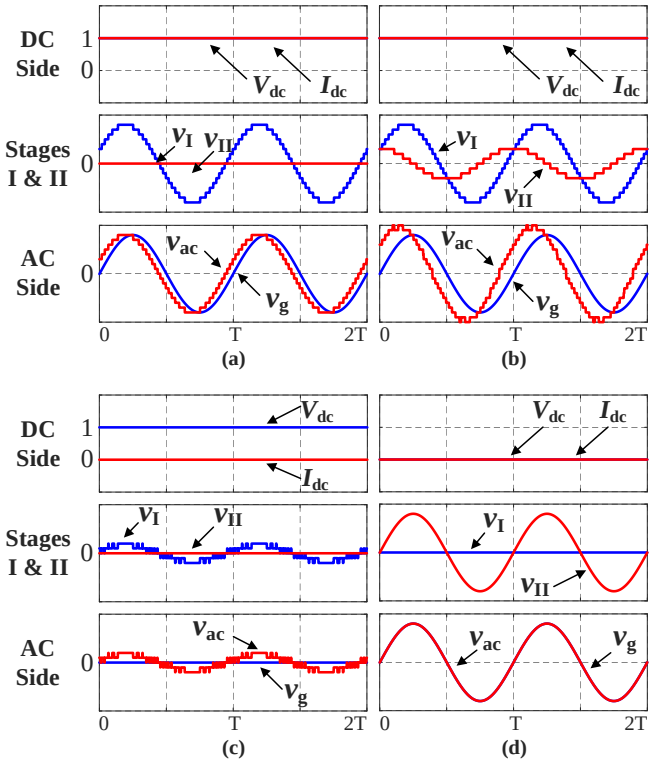

Fig. 4. T-MMC conceptual waveforms (in pu) in normal and faulty network cases. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

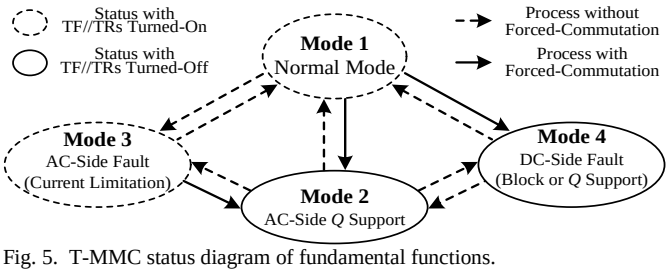

Fig. 5. T-MMC status diagram of fundamental functions.

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1) Mode 1: By operating Stage-I as a conventional HB MMC, and with all Stage-II thyristors on, the T-MMC functions in the 'normal' mode. As shown in Fig. 4(a), Stage-I is responsible for generating the ac-side voltage required by the grid-connected controllers [6]. To avoid short circuit, FB SMs of Stage-II are not allowed to actively generate voltages in this mode, except for thyristor turn-off commutation. The conducting capability of thyristors compared to that of IGBTs minimizes losses of Stage-II. Accordingly, T-MMC affords similar operation efficiency to conventional HB MMC (Stage-I). The voltage drop across Stage-II is neglected in the conceptual waveforms in Fig. 4(a).

2) Mode 2: When the reactive power (voltage) support is needed by the ac grid, T-MMC is able to increase the ac-side voltage amplitude, thus avoiding Stage-I over-modulation. The T-MMC behavior during ac-side Q support is illustrated in Fig. 4(b), where both stages contribute to generating the ac-side voltage v_{ac} (the vector sum). As PCC active power is still provided by Stage-I, dc-side power remains at 1pu. In this mode, all thyristors of Stage-II must be off so that the FB SM string of Stage-II acts as a series-connected cascaded H-bridge STATCOM. Theoretically, the operation of the two stages is not independent; therefore Stage-II voltage and current vectors are controlled to be orthogonal for the steady-state energy balance.

3) Mode 3: AC fault ride-through techniques with VSCs are well investigated [1]. When a worst-case solid ac-side fault occurs, T-MMC Stage-I reduces its ac output voltage to limit the fault current, similar to the behavior of a conventional HB MMC. Illustrative waveforms are shown in Fig. 4(c), where Stage-I controls reactive current and Stage-II is bypassed (v_{II} is assumed to be zero). In terms of a three-phase system, negative sequence current elimination is also feasible in asymmetrical ac fault cases [39].

4) Mode 4: Fig. 4(d) illustrates T-MMC dc fault isolation capability under the worst dc-side fault condition. Stage-I upper and lower arms are bypassed; thus, v_I is negligibly small. With the same voltage rating as Stage-I, Stage-II can safely isolate the dc and ac sides by the FB SM string barrier (all thyristors and IGBTs are off). Then no ac-side current can sink into the dc side. Stage-II can also operate as a STATCOM to provide supportive Q for the tied-grid.

Fig. 5 shows T-MMC status for each of the four functions. AC-side reactive power support and dc fault isolation rely on the active operation of Stage-II, and the transitions to them involve prompt commutation of TSGs.

III. The THYRISTOR-SM GROUPS (TSGS)

Various natural and forced commutation methods exist to turn off thyristors, and here the parallel voltage forced-commutation is implemented within each TSG, where the FB SMs can be configured as parallel commutating voltage sources [40]. An illustrative TSG schematic with one FB SM (F=1) is depicted in Fig. 6(a). The thyristor forced-commutation is achieved by the manipulation of the FB SM and thyristors, as the procedure shown in Fig. 6(b). The

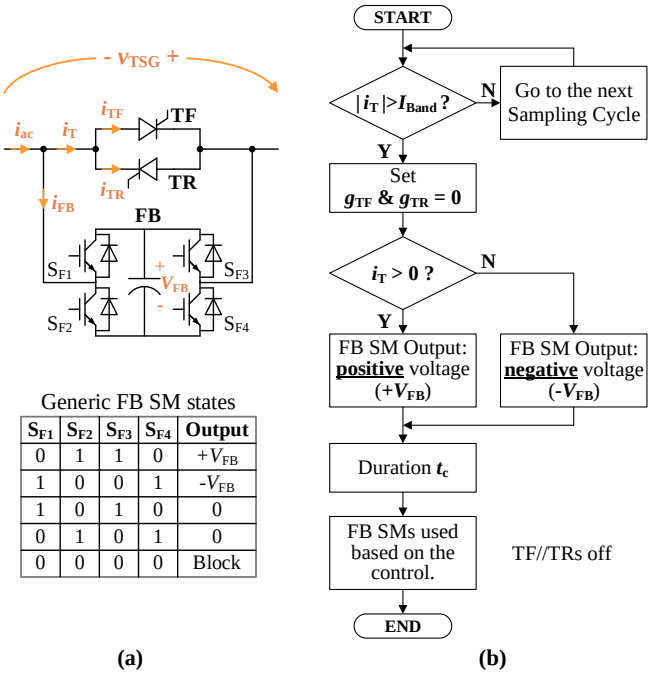

Fig. 6. Thyristor-commutation illustration. (a) Schematics of the TSG (F=1) and generic FB SM states. (b) Procedure flow chart.

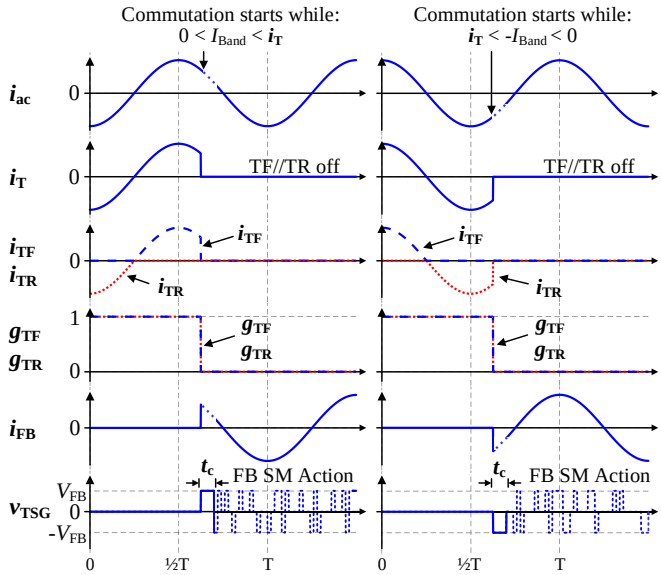

Fig. 7. Descriptive waveforms (in pu) of the thyristor-commutation process.

essential condition is a reverse voltage applied to the on-state thyristor. By providing the FB SM path with lower impedance (a parallel voltage), the ac current is transferred from the thyristor path to the FB SM path. Given a thyristor turn-off time t_q, a parallel voltage duration t_c longer than t_q is required. Practically, to avoid incorrect detection of the ac current zero-crossing point, a dead-band (I_{Band}, larger than the current measurement tolerance) is used. Forced-commutation process waveforms are illustrated in Fig. 7, where the duration t_c is exaggerated for illustration, and g_{TF} and g_{TR} are the triggering signals of TF and TR respectively. Enabled g_{TF} and g_{TR}

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TABLE I. Comparison of Various Typical MMCs

	HB MMC	Mixed-Cell MMC (HB:FB = 1:1)	Mixed-Cell MMC (HB:FB = 1:2)	FB MMC	T-MMC
DC-Side voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
SM No. per phase	$2N$	$2N$	$2N$	$2N$	$2N$ (Stage-I); MF (Stage-II)
SM rated voltage	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N (Stage-I); $½V_{dc}/(MF)$ (Stage-II) [1]
IGBT/Diode No. per phase	$4N$	$6N$	$20N/3$	$8N$	$8N$ (if $MF = N$) [2]
Thyristor No. per phase [8]	$4N$	$4N$	$4N$	$4N$	$4N + 2M$
Cost grade	Low [3]	Medium [3]	Medium [3]	High [3]	High
IGBT/Diode No. in current path	$2N$	$3N$	$10N/3$	$4N$	$2N$
Thyristor No. in ac current path	0	0	0	0	M
Operation losses	Low	Medium	High	Very high	Low, in normal mode.
DC fault isolation	No	Yes	Yes	Yes	Yes
Maximum converter ac voltage	$½V_{dc}$	$½V_{dc}$ [3]	$½V_{dc}$ [3]	$½V_{dc}$ [3]	V_{dc} [4]
Performance of ac-side Q-support in normal cases	Acceptable	Acceptable [5]	Acceptable [5]	Acceptable [5]	Excellent [4]
AC-Side Q-support during dc fault	No	Yes	Yes	Yes	Yes

[1]: Assuming $V_I = V_{II}$; thus, ac voltage synthesis and Stage-II ESE integration becomes more flexible.
[2]: Assuming $V_I = V_{II}$ and $MF = N$.
[3]: More SMs and additional investment are required for a higher ac voltage.
[4]: Assuming $V_I = V_{II}$. This is achieved by operating stages I and II simultaneously.
[5]: More SMs are required to achieve higher performance.

indicate that the gate drivers are turned on to provide gate currents, whereas disabled g_{TF} and g_{TR} indicate zero gate current. As the FB SM capacitor is discharging during the interval t_c, with ideal switches (zero conduction and switching losses), the capacitor voltage variation is:

$$C_{FB} \times \Delta V_{FB} = \int_{t}^{t+t_c} i_{ac}(t)dt \tag{1}$$

where ΔV_{FB} is the capacitor voltage variation due to the commutation process and $i_{ac}(t)$ is the instantaneous ac current.

Presently, high-power converter grade thyristors have significant re-applied dv/dt capabilities (kV/μs), and maintaining circuit parameters under limits is not difficult. Additionally, RCD snubber circuits can be used to avoid the erroneous thyristor reactivation caused by the dv/dt. Using partial SMs or a specific SM within a TSG for commutation is also feasible. On the other hand, thyristors have high on-state di/dt ratings (kA/μs), which are sufficient for dynamic performance. For the generic grid-connected scenario in Fig. 3, the instantaneous di/dt of the turned-on thyristors within Stage-II is:

$$\frac{di}{dt} = \frac{v_I - Ri_{ac} - v_g}{L} \tag{2}$$

During commutation, the ac current is temporarily out of control, with a maximum possible deviation of:

$$\left|\Delta I_{ac}\right|_{max} = t_c \frac{V_{II} + RI_{ac}}{L} \tag{3}$$

where I_{ac} is the ac current magnitude. Fortunately, the current control variable trajectory is slightly influenced due to the short duration t_c and inductive impedance of the ac bus (in both the internal arms and external load).

Consequently, Stage-II is able to switch between the thyristor-based efficient state and the FB SM based active state, depending on the converter mode requirement. However, compared with the FB and mixed-cell MMCs, the T-MMC avoids improving the dc fault tolerance ability by simply inserting FB SMs into the main conduction path. With TSGs, the T-MMC retains dc fault ride-through capability without compromising normal operation efficiency. Thus, this paper provides an effective solution to the mentioned trade-off between fault-blocking competency and operation efficiency of a converter. A comparison of different typical MMCs is given in Table I, considering semiconductor usage, quantitative losses, critical features, etc., [5], [7].

IV. T-MMC Based ESS and Its Additional Functions

Among various electrical energy storage technologies, battery and supercapacitor are two types which offer high energy and power density features respectively [29]. As T-MMC SMs can perform flexible control and management in terms of voltage balancing, state-of-charge (SoC), health, etc., the distributed deployment of rechargeable batteries and/or supercapacitors (SCs) is applicable [41], [42]. Although, from the system inertia point of view, it is desirable to equip the converter with as much ESEs as possible, integrating ESEs into the Stage-I is not necessary for the fulfillment of additional functions. Integrating proper ESEs into the Stage-II is essential, and the proposed Stage-II is friendly to the splitting ESE integration. From Section II, the FB SMs voltage level V_{FB} can be adjusted by M and F (and K) to suit commercially available ESEs, of which the voltage level is usually obtained by a series-connection of small cells. Despite an increased cost, the T-MMC topology shown in Fig. 2 allows galvanic isolation of ESEs.

A. Additional Security Functions

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The grid-connected system model in Fig. 8 shows a power path to the ESEs. As a result, flexible power flow management is achieved, which can improve converter resilience against ac/dc faults and other severe disturbances. With added energy storage, Stage-II can partake in active power exchange. The T-MMC based ESS is able to simultaneously provide enlarged *P-Q* support for the ac side due to the independent Stage-II. In addition, power systems may suffer from sudden power changes during ac network faults or consumption/generation fluctuation. With appropriately sized ESEs, the power relationship between dc and ac sides can be decoupled by the converter, leading to a significantly increased security margin of the tied systems.

Generally, the most severe fault case is that one side completely loses its power due to the solid fault. If the ESE within Stage-II has a sufficient power/energy rating, any power pause in the dc/ac side caused by the ac/dc side fault can be eliminated. Single-phase conceptual waveforms are shown in Fig. 9. When a worst-case solid ac-side fault occurs, the T-MMC ac-side output voltage v_{ac} is reduced under control. In Fig. 9(a), Stage-I maintains its original power conversion (P_{dc} is maintained), whereas Stage-II operates to exchange power with the Stage-I ($P_{ESE} = P_{dc}$). This is a special case of ac-side power support. Under the worst dc-side fault condition, Stage-I upper and lower arms are bypassed, and Stage-II generates ac voltage to provide *P-Q* support ($P_{ESE} = P_{ac}$), as shown in Fig. 9(b).

The status of the T-MMC based ESS is shown in Fig. 10, where Stage-II thyristors are turned-off in modes 2 to 4 to allow the active operation of the FB SMs.

B. The ESE within Stage-II

Stage-II performance depends on the characteristics of the integrated ESEs. For example, when a fault occurs, transient power support is mainly determined by the ESE power capability. Currently, the SC is an attractive choice due to high power capability and long lifetime; an example is shown in Fig. 11, where the FB SM is equipped with an SC module of N_S series and N_P parallel connected SC cells [43]. Usually, due to the intrinsic time constant of SCs, a shunt connection with conventional electrolytic and/or film/paper capacitors (with the lower ESR and longer lifetime) results in an efficient configuration [44].

Sizing of the Stage-II ESE can be evaluated, assuming:

1) SC modules: All Stage-II 3×*M*×*F* FB SMs are integrated with the same rated SC modules;

2) SC cells: Cells inside the SC module are balanced in terms of voltages and currents, whereas the capacitance and ESR of cells (C_{cell} and R_{cell} respectively) are equal and constant; and

3) Conventional capacitors: The ESR and stored energy of the conventional capacitors are negligible compared with those of the SC, whereas the current pulse due to switching action is sourced by conventional capacitors.

There are some design factors to be considered:

1) Rated voltage: The minimum number of series-connected cells within one SC module N_S is determined by:

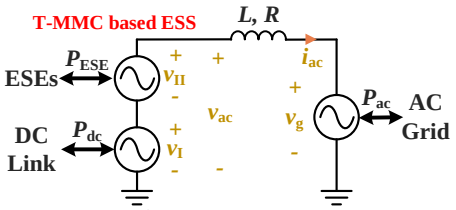

Fig. 8. Analytical model of a grid-connected system with T-MMC based ESS.

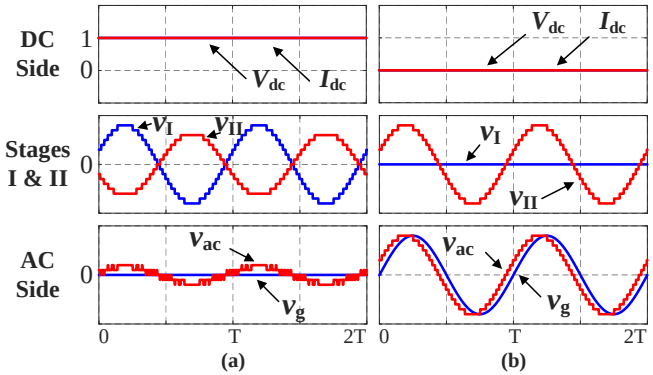

Fig. 9. T-MMC conceptual waveforms (in pu) with sufficient ESEs in network faults. (a) Mode 3. (b) Mode 4.

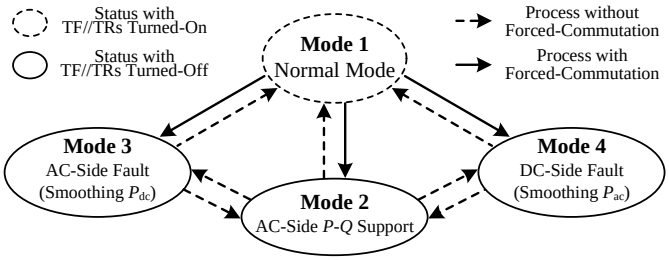

Fig. 10. Status diagram of the T-MMC based ESS with additional functions.

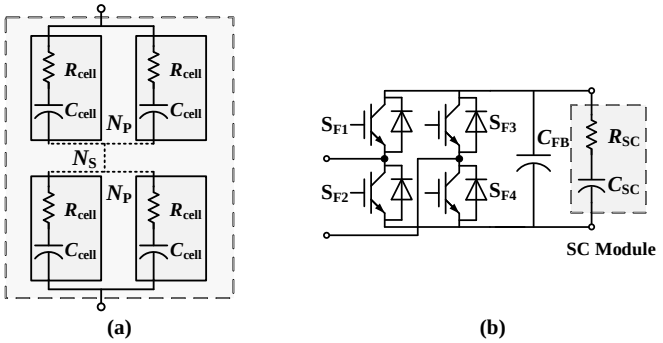

Fig. 11. ESE example. (a) Simplified model of an SC module. (b) FB SM with an SC module.

$$N_S \geq V_{FB}/V_{cell} \tag{4}$$

where V_{FB} is the steady-state voltage set point of the FB SM and V_{cell} is the SC cell rated voltage.

2) Available energy and absolute maximum voltage: The number of parallel-connected cells within one SC module is:

$$N_{P(1)} \geq \frac{2P_{ESE}T_{ESS}}{3MFN_SC_{cell}V_{cell}^2[1-(1-\delta)^2]} \tag{5}$$

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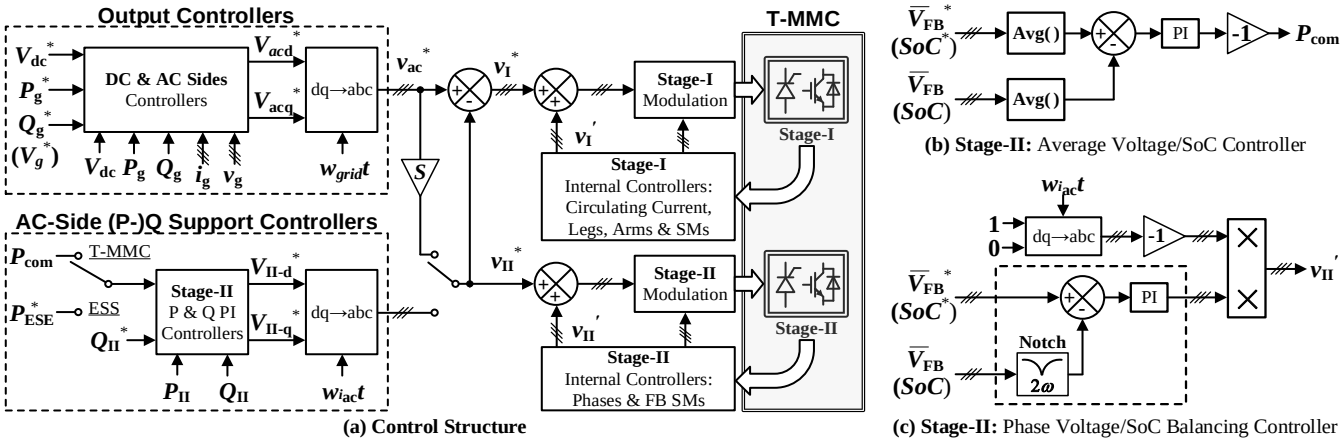

Fig. 12. T-MMC control system for grid-connected applications.

where T_{ESS} is the ESS full-power operation duration, and δ is the SC maximum charge/discharge depth, which for safety should be restricted to:

$$\delta \le \hat{V}_{cell}/V_{cell} - 1 \tag{6}$$

where $\hat{V}_{cell}$ is the SC cell absolute maximum voltage.

3) Absolute maximum current: From an over-current protection perspective, another boundary is:

$$N_{P(2)} \ge KI_{ac}/\hat{I}_{cell} \tag{7}$$

where K = 1 or the transformer turning ratio, depending on the topology, and $\hat{I}_{cell}$ is the SC cell absolute maximum current.

4) SM voltage drop: The SC ESR and SM semiconductors lead to voltage drops, which may affect Stage-II output waveform synthesis. Hence, assuming a fixed on-state semiconductor voltage drop $V_{SEMI\text{-}FB}$, N_P should also satisfy:

$$N_{P(3)} \ge \frac{KI_{ac}R_{cell}N_S}{V_{FB} - V'_{FB} - 2V_{SEMI-FB}} \tag{8}$$

where V'_{FB} is the acceptably minimum value of the FB SM positive output voltage.

Based on the constraints in (5), (7) and (8), the minimum number of parallel-connected cells within one SC module N_P is:

$$N_P = \max(N_{P(1)}, N_{P(2)}, N_{P(3)}) \tag{9}$$

With the determined N_S and N_P, Stage-II ESE energy capability E_{ESE} can be calculated as:

$$E_{ESE} = 1.5MFN_SN_PC_{cell}V^2_{cell} \tag{10}$$

V. Control Strategy

Due to T-MMC topology complexity, the control system is suggested to be hierarchical, including output control (for dc and/or ac sides), stage-level control, and inner-stage control. The inner-stage control for Stage-I includes MMC circulating current control and leg, arm and SM level control, whereas Stage-II internal control involves phase and SM level control.

The control structure for dc/ac grid-connected applications is shown in Fig. 12(a), where the output controllers control the ac grid active and reactive powers (extra dc-side voltage control loop is based on the active power regulation). Various VSC grid-forming or grid-following control schemes are applicable for different scenarios. As a result, a T-MMC three-phase output voltage reference v_{ac}^* is obtained.

Stage-level control coordinates the operation of two stages, and therefore takes responsibility to tackle abnormal cases. In Fig. 12(a), variable S is assigned to be '0' (no dc fault) or '1' (dc pole-to-pole fault), reflecting the dc network health status. Further functions, including pole-to-ground fault detection or power-sharing between stages, are also feasible. Normally, the Stage-I ac voltage reference (v_I^*) equals v_{ac}^*, whereas that of the Stage-II (v_{II}^*) is zero (hardware-wise, TSG thyristors are turned on), indicating the normal mode in Fig. 5 or Fig. 10. In general, when a dc fault occurs (S = 1), Stage-II can either block the dc/ac sides or generate the ac voltage (using v_{ac}^*) under the regulation of the ac-side output controllers. If the ESEs are integrated into Stage-II, ac grid active power can be maintained. The ac-side (*P*-)*Q* support controllers are enabled

TABLE II. Simulation Parameters

	Parameters	Rating
DC side	DC-link voltage	40kV
	DC cable distance	10km
	DC cable (T-model) inductance	150uH/km
	DC cable (T-model) resistance	11mΩ/km
	DC cable (T-model) capacitance	200nF/km
AC side	AC grid frequency	50Hz
	AC grid voltage	33kV
	Transformer ratio	20/33kV
	Transformer leakage inductance	0.18pu
Stage-I	HB SM number per arm N	20
	HB SM rated voltage	2kV
	HB SM capacitance C_{HB}	6.7mF
	Arm inductance L_1	0.2pu
Stage-II (ESS)	TSG number per phase M	10
	FB SM number per TSG F	4
	FB SM rated voltage	0.55kV
	Thyristor turning-off time t_q	500us
	Forced-commutation duration t_c	700us
	FB SM capacitance (without ESE) C_{FB}	18mF
	FB SM capacitance (with ESE) C_{FB}	3mF
	SC cell type	BCAP0310
	Series cell number per module N_S	204
	Parallel cell number per module N_P	8
	SC module capacitance C_{SC}	12.15F
	SC module ESR R_{SC}	56.1mΩ

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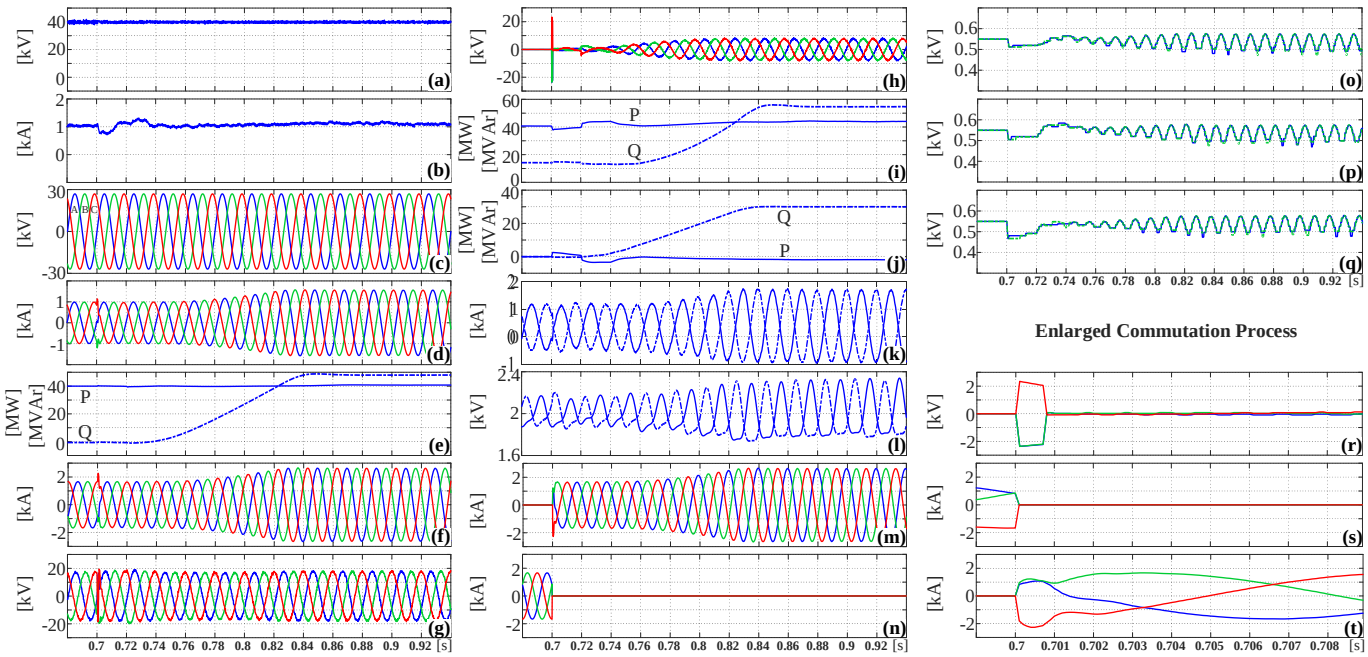

Fig. 13. T-MMC simulation in the ac-grid *Q* support mode. (a) T-MMC dc-side voltage. (b) T-MMC dc-side current. (c) PCC voltage. (d) PCC current. (e) PCC powers. (f) T-MMC ac-side current. (g) Stage-I ac-side voltage. (h) Stage-II output voltage. (i) Stage-I powers. (j) Stage-II powers. (k) Phase-A Stage-I arm currents. (l) Phase-A Stage-I arm average capacitor voltages. (m) Stage-II TSG_1 FB SM path current. (n) Stage-II TSG_1 thyristor path current. (o) Phase-A Stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (p) Phase-B stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (q) Phase-C stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (r) Stage-II TSG_1 output voltage. (s) Stage-II TSG_1 thyristor path current, and (t) Stage-II TSG_1 FB SM path current.

and selected when ac-side support (including active power support and ancillary services) or Stage-II stored energy management is required. As shown in Fig. 12(a), Q_{II}^* can be used to make Stage-II contribute to voltage support, whereas P_{com} (to compensate power losses in ac-side *Q* support mode) or P_{ESE}^* (to maintain continuous *P* support with ESEs) is configured to achieve active power exchange. Fig. 12(b) shows the Stage-II overall capacitor voltage/SoC controller, which is used to adjust the stored energy within the FB SMs.

The Stage-I internal control schemes are selected as in [6] and [45]. An inter-phase voltage/SoC balancing controller is shown in Fig. 12(c), where notch filters are adopted to suppress potential second-order harmonics without delay, and fundamental frequency voltage injection ensures active power (voltage/SoC) regulation.

Centralized and distributed SM-level voltage/SoC balancing techniques can be found in [2] and [3].

VI. Simulation Evaluation

A T-MMC, with its dc side connected to a voltage-controlled dc link through a short cable and its ac side connected to a stiff ac grid through a Δ-Y interfacing transformer, is simulated using MATLAB/Simulink, with parameters listed in Table II. A conventional grid-connected control structure, with inner vector current loops, outer *P*-*Q* loops and PLL, is adopted. In the normal case, the Stage-I is controlled to inject 40MW active power into the PCC at unity power factor, and Stage-II TF//TRs are on.

A. T-MMC

In this subsection, T-MMC performances for ac-side reactive power support and dc fault ride-through are presented, with the waveforms shown in Fig. 13-15.

Fig. 13 shows T-MMC transient behavior when the ac grid needs voltage support from 0.7s. After thyristor-commutation, the output and activated ac-side *Q* support controllers operate together from 0.72s, and the PCC reactive power ramps up to 48MVAr approximately, see Fig. 13(e). The voltage contribution of each stage is shown in Fig. 13(g)-(j), where Stage-II increases ac voltage synthesis while Stage-I maintains the original ac-side voltage amplitude (without over-modulation). With a constant PCC voltage, the three-phase currents are increased due to the increased *Q*, whereas the dc and active powers are slightly influenced, as shown in Fig. 13(a)-(f). Stage-I arm currents and SM voltage ripple increase, as displayed in Fig. 13(k) and (l). Stage-II ac current is commutated from the thyristor paths to the FB SM paths after 0.7s, and Stage-II capacitor voltages are controlled and balanced, as shown in Fig. 13(m)-(t). Due to thyristor forced-commutation, the ac current is temporarily uncontrolled, with a small deviation, see Fig. 13(r)-(t). The fluctuation of the active power of stages is due to the regulation of Stage-II capacitor voltages.

Fig. 14 shows T-MMC dc fault blocking capability. A pole-to-pole solid short-circuit dc fault is applied at 0.4s and cleared after 140ms, and thus voltage and current of T-MMC dc-side terminal fall to zero, as depicted in Fig. 14(a) and (b). Thyristor and FB SM paths of Stage-II are turned-off and blocked respectively, and Stage-I SMs are also blocked, as shown in Fig. 14(k)-(q). With the assistance of T-MMC Stage-II, inrush current from the ac side into dc side is prevented,

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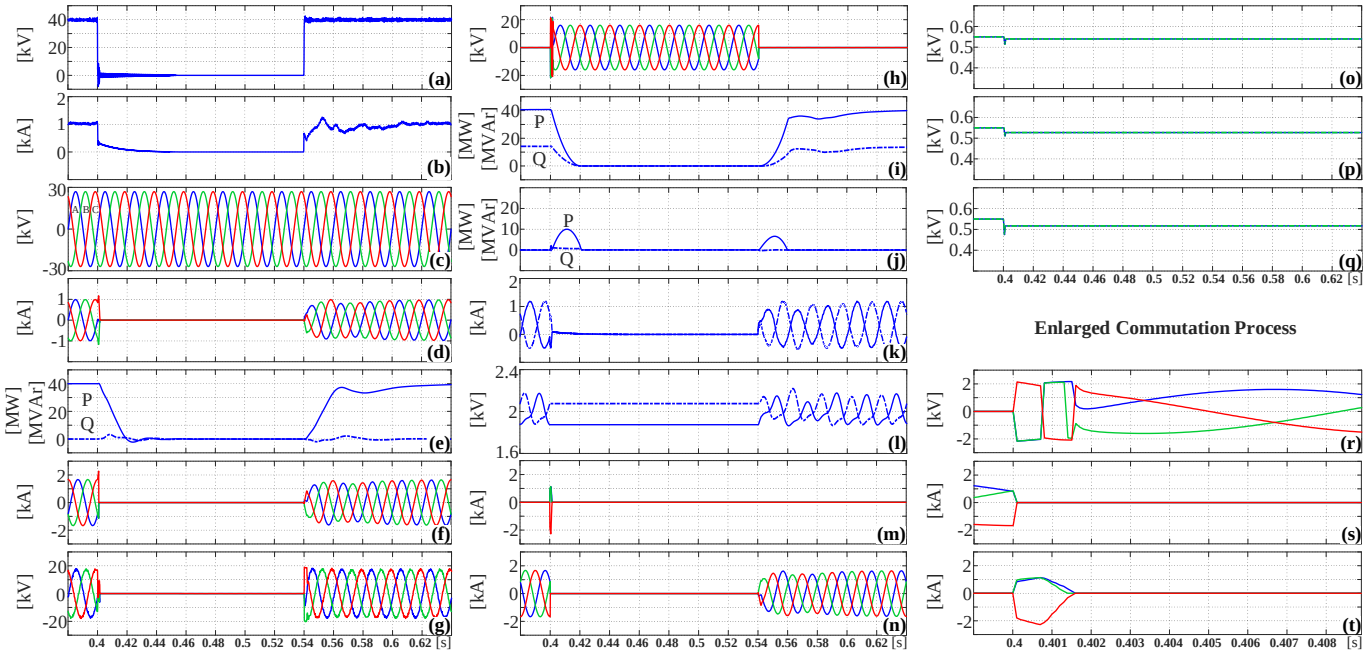

Fig. 14. T-MMC simulation in a dc-link fault case (block). (a) T-MMC dc-side voltage. (b) T-MMC dc-side current. (c) PCC voltage. (d) PCC current. (e) PCC powers. (f) T-MMC ac-side current. (g) Stage-I ac-side voltage. (h) Stage-II output voltage. (i) Stage-I powers. (j) Stage-II powers. (k) Phase-A Stage-I arm currents. (l) Phase-A Stage-I arm average capacitor voltages. (m) Stage-II TSG_1 FB SM path current. (n) Stage-II TSG_1 thyristor path current. (o) Phase-A Stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (p) Phase-B stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (q) Phase-C stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (r) Stage-II TSG_1 output voltage. (s) Stage-II TSG_1 thyristor path current, and (t) Stage-II TSG_1 FB SM path current.

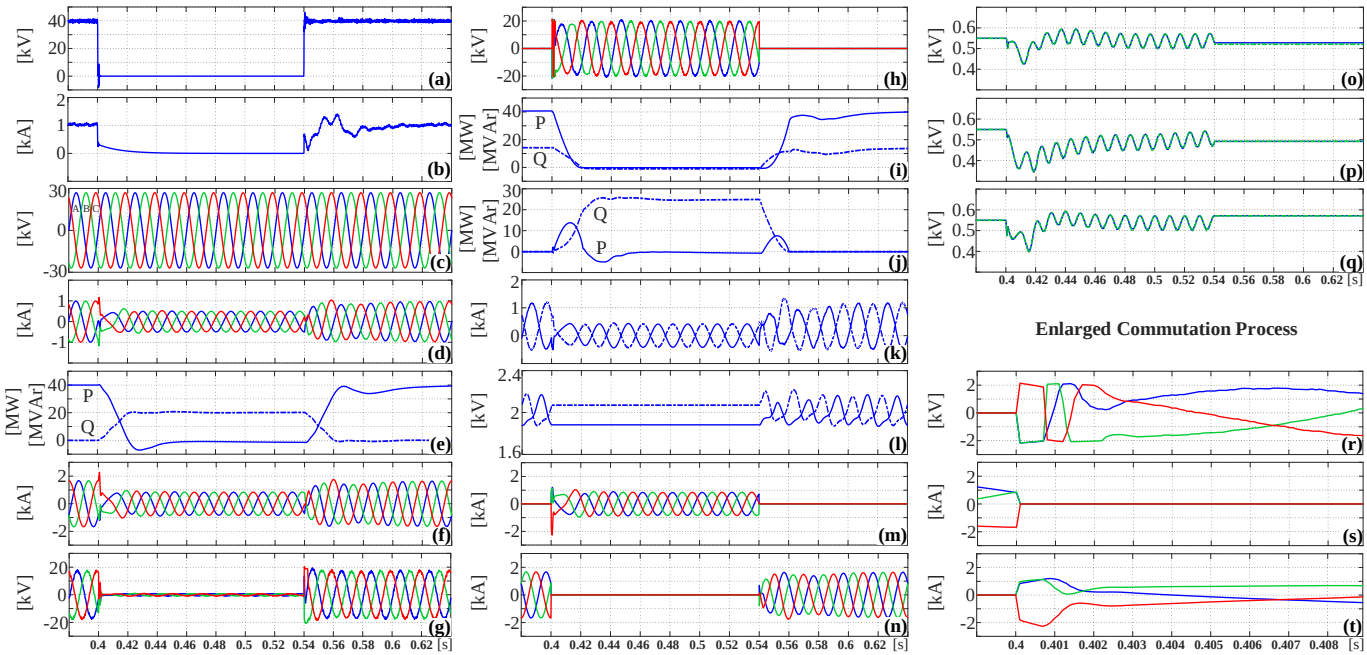

Fig. 15. T-MMC simulation in a dc-link fault case (*Q* support). (a) T-MMC dc-side voltage. (b) T-MMC dc-side current. (c) PCC voltage. (d) PCC current. (e) PCC powers. (f) T-MMC ac-side current. (g) Stage-I ac-side voltage. (h) Stage-II output voltage. (i) Stage-I powers. (j) Stage-II powers. (k) Phase-A Stage-I arm currents. (l) Phase-A Stage-I arm average capacitor voltages. (m) Stage-II TSG_1 FB SM path current. (n) Stage-II TSG_1 thyristor path current. (o) Phase-A Stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (p) Phase-B stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (q) Phase-C stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (r) Stage-II TSG_1 output voltage. (s) Stage-II TSG_1 thyristor path current, and (t) Stage-II TSG_1 FB SM path current.

and ac-side voltage stress transfers to Stage-II, see Fig. 14(c)-(j). Fig. 14(r)-(t) depict the thyristor-commutation process.

Fig. 15 demonstrates T-MMC reactive power support function during a dc fault. With the previous fault condition, simulation waveforms in Fig. 15(d)-(h) show that after thyristor-commutation, the T-MMC (Stage-II, specifically) generates ac voltage to support the ac side (with ac grid reactive power equals 20MVAr), rather than eradicates ac current. Stage-I bypassed arms become part of the ac bus while its SMs remain blocked, see Fig. 15(i), (k) and (l). Fig.

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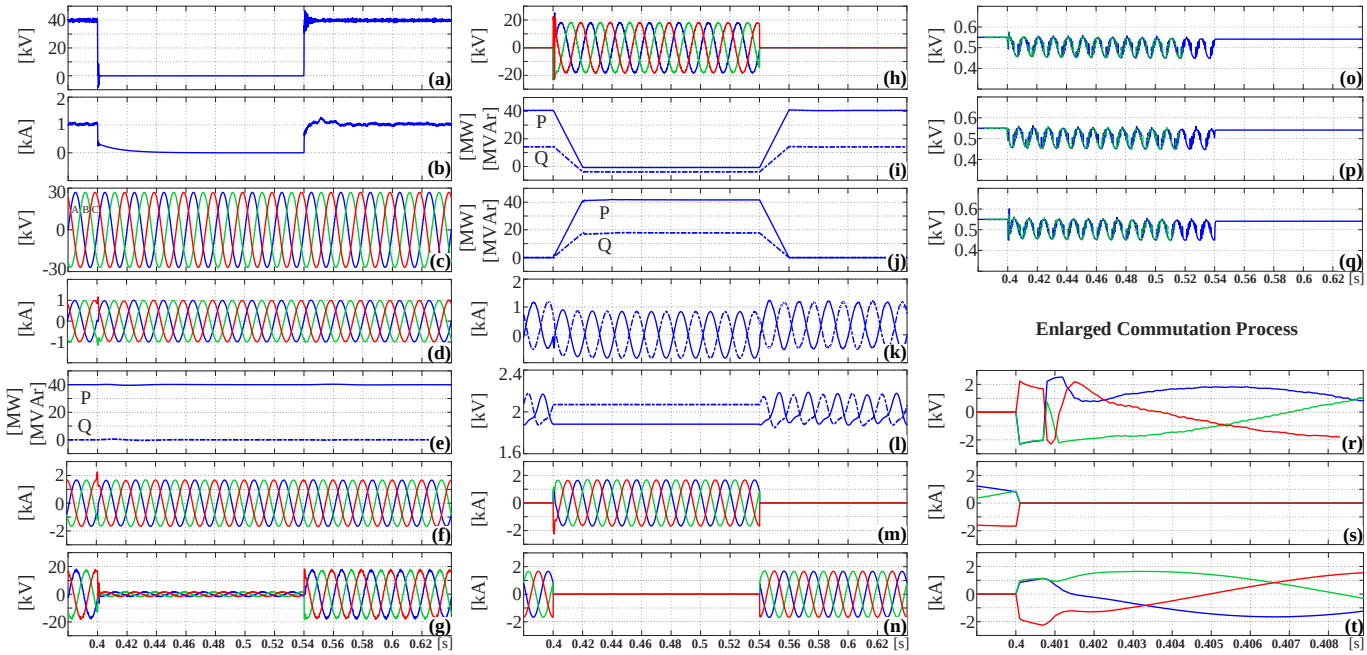

Fig. 16. Simulation of T-MMC based ESS in a dc-link fault case. (a) T-MMC dc-side voltage. (b) T-MMC dc-side current. (c) PCC voltage. (d) PCC current. (e) PCC powers. (f) T-MMC ac-side current. (g) Stage-I ac-side voltage. (h) Stage-II output voltage. (i) Stage-I powers. (j) Stage-II powers. (k) Phase-A Stage-I arm currents. (l) Phase-A Stage-I arm average capacitor voltages. (m) Stage-II TSG_1 FB SM path current. (n) Stage-II TSG_1 thyristor path current. (o) Phase-A Stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (p) Phase-B stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (q) Phase-C stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (r) Stage-II TSG_1 output voltage. (s) Stage-II TSG_1 thyristor path current, and (t) Stage-II TSG_1 FB SM path current.

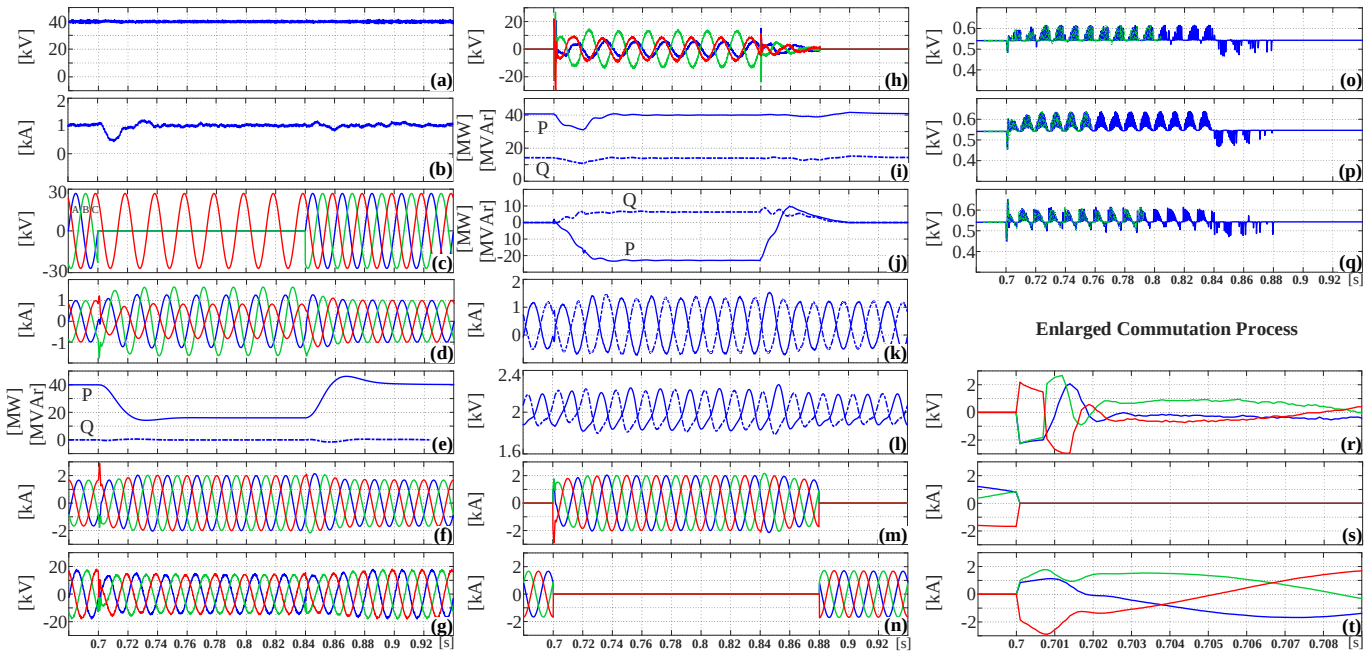

Fig. 17. Simulation of T-MMC based ESS in an ac-grid fault case. (a) T-MMC dc-side voltage. (b) T-MMC dc-side current. (c) PCC voltage. (d) PCC current. (e) PCC powers. (f) T-MMC ac-side current. (g) Stage-I ac-side voltage. (h) Stage-II output voltage. (i) Stage-I powers. (j) Stage-II powers. (k) Phase-A Stage-I arm currents. (l) Phase-A Stage-I arm average capacitor voltages. (m) Stage-II TSG_1 FB SM path current. (n) Stage-II TSG_1 thyristor path current. (o) Phase-A Stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (p) Phase-B stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (q) Phase-C stage-II TSG_1 $SM_{1\&2}$ capacitor voltages. (r) Stage-II TSG_1 output voltage. (s) Stage-II TSG_1 thyristor path current, and (t) Stage-II TSG_1 FB SM path current.

15(j) and (o)-(q) show that Stage-II operates as a STATCOM connected to the PCC, where the active power exchange regulates the capacitor voltages, and reactive power output is utilized for PCC *Q* support.

B. T-MMC Based ESS

In this subsection, the simulated behavior of T-MMC based ESS, in dc and ac fault cases, are presented in Fig. 16 and 17 respectively.

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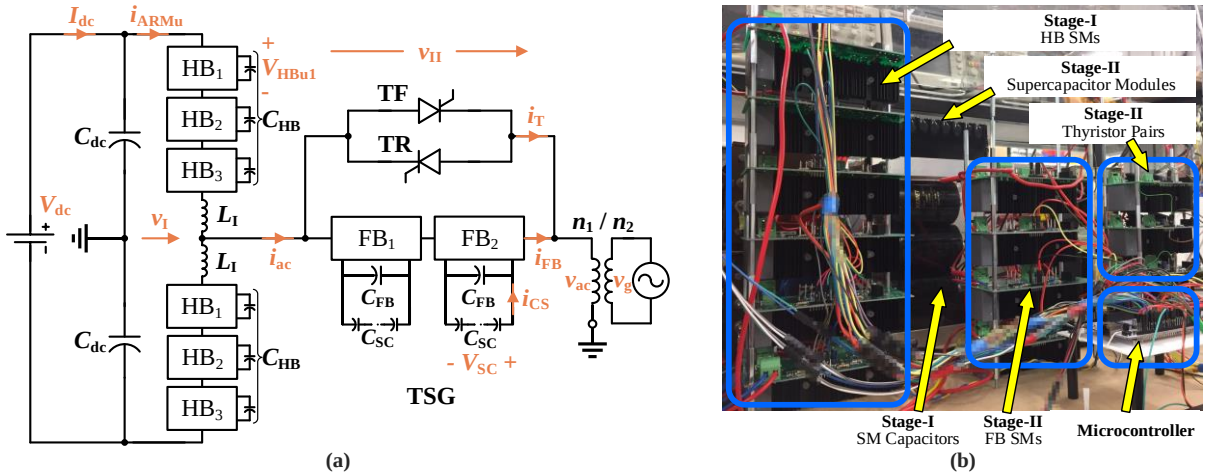

Fig. 18. Experimental prototype of the proposed T-MMC integrated with SCs. (a) Schematics. (b) Photograph.

With a pole-to-pole solid short-circuit dc fault from 0.4s to 0.54s, the T-MMC based ESS controls ac-grid current and also maintains continuous active power injection, as shown in Fig. 16(a)-(f). With Stage-I bypassed, this control is achieved by the independent Stage-II, which is able to synthesize ac voltage and exchange active power with the PCC, see Fig. 16(h)-(j). During the dc fault, phase-A Stage-I common-mode currents are reduced to zero and SMs are blocked, while Stage-II SCs discharge, as shown in Fig. 16(k)-(q). The Stage-II thyristor turning-off process, after 0.4s, is illustrated in Fig. 16(r)-(t).

A solid short-circuit ac fault (phase A and B) occurs at 0.7s, and the T-MMC based ESS can eliminate the PCC negative sequence current components and smooth the dc power, as shown in Fig. 17(a)-(f). Stages I and II operate simultaneously, and Stage-II absorbs a portion of the active power from Stage-I to match the power imbalance, see Fig. 17(g)-(l). SCs within Stage-II FB SMs are charging, as shown in Fig. 17(m)-(q). Fig. 17(r)-(t) show the discussed thyristor forced-commutation process.

VII. Experimental Results

A single-phase prototype with ESE integration is used to verify the main functions of the proposed T-MMC, with the hardware schematics, photograph and parameters shown in Fig. 18 and Table III. The voltage and current variables for the waveforms are measured as indicated in Fig. 18(a) and Fig. 19. The converter is controlled to transfer rated power from the dc to ac side, whereas the control system is executed by an Arm Cortex-M7 processor, including the sorting-based algorithm for the SM voltage balancing.

Fig. 20 shows T-MMC waveforms during the normal operation. In Fig. 20(a)-(d), converter ac-side current (with an amplitude of 20A) is near sinusoidal and in phase with the grid voltage, injecting rated power at unity power factor. Stage-I takes over ac-side voltage generation (with most switching harmonics suppressed by the ac bus inductive impedance), whereas the thyristors (TF and TR) are maintained on to bypass the IGBT-based FB SMs, see Fig. 20(e)-(h). With the voltage drop across Stage-II being about 1V (due to the superior conducting characteristics of thyristors), Stage-II conduction losses are minimized in this normal mode, see Fig. 20(f)-(h). The upper arm current and HB_1 SM capacitor voltage of Stage-I are shown in Fig. 20(i) and (k), indicating the circulating current is suppressed and SM voltages are controlled by the inner-stage controllers. As the FB SMs of Stage-II are bypassed, SC current is zero; hence the SC voltage is constant, see Fig. 20(j) and (l).

In order to verify the ac-side voltage boost ability of the proposed T-MMC, a significantly increased interfacing inductance, which would require an extra inductive Q, is used as illustrated in Fig. 19.

The experimental waveforms in Fig. 21(a)-(e) show that the T-MMC (Stage-I) maintains its active power conversion, whereas both stages are activated, contributing to generation of the increased ac-side voltage, see Fig. 21(f)-(j). As a result, an enlarged ac-side output voltage ($v_{ac} = v_I + v_{II}$) is synthesized (approximately 180V peak-to-peak), whereas both stages

TABLE III. Hardware Parameters

	Parameters	Rating
DC/AC Sides	Rated Power	500W
	DC-Side voltage V_{dc}	120V
	DC link capacitance C_{dc}	6.8mF
	AC grid rms voltage v_g	240V
	AC transformer leakage	250uH
	AC transformer ratio n_1/n_2	36/240
Microcontroller	Modulation type	PWM-PD
	Switching frequency	2kHz
	Sampling frequency	10kHz
Stage-I	HB SM rated voltage	40V
	HB SM capacitance C_{HB}	3.8mF
	HB SM IGBT type	IRG7PH35UD1-EP
	Arm inductance L_I	3mH
Stage-II (ESS)	FB SM rated voltage	32V
	FB SM capacitance C_{FB}	2mF
	FB SM IGBT type	IRG7PH35UD1-EP
	Thyristor (TF//TR) type	TM8050H-8W
	Commutation duration t_c	300us
	SC cell type	BCAP0100
	Series cell No. per module N_S	18
	Parallel cell No. per module N_P	1
	SC module capacitance C_{SC}	5.55F

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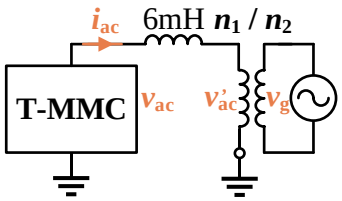

Fig. 19. Schematics for the ac-side voltage boost case.

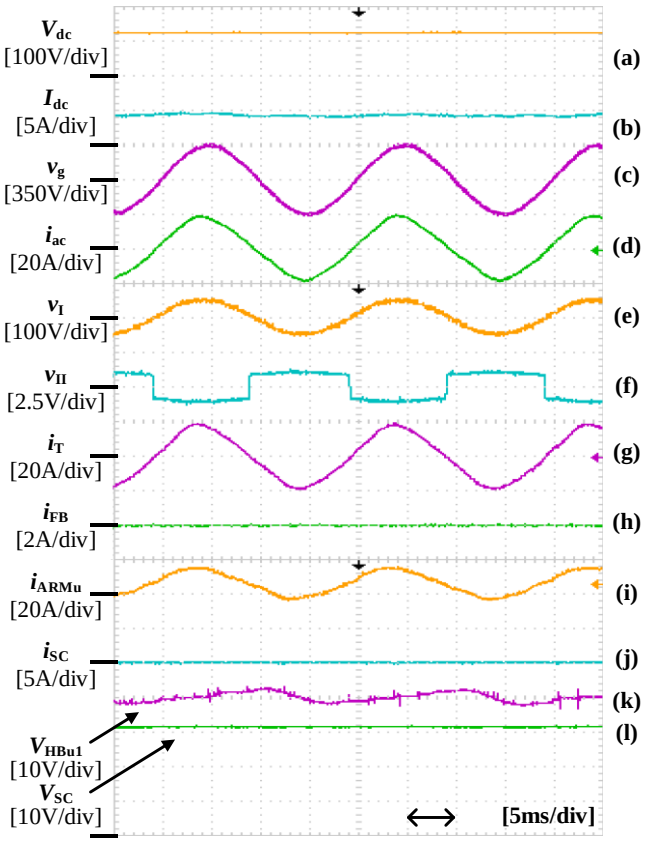

Fig. 20. T-MMC waveforms in the normal mode.

operate without over-modulation. Stage-I upper arm current and HB_1 SM capacitor voltage, which are regulated, are shown in Fig. 21(k) and (n). As stage-II only provides reactive power, the mean SC charging current is zero and the SC voltage remains in steady-state (with minor ripple due to the SC internal resistance), see Fig. 21(l) and (m).

Fig. 22 demonstrates the thyristor-commutation process of the TSG in Stage-II. When the ac current is positive (conducted by the TF), the forced-commutation is achieved when the FB SM generates a positive voltage for a duration t_c. Then, with TF turned-off, the ac current is commutated from the thyristor path to the FB SM path. The process for TR commutation is shown for the negative i_{ac} case. The ac current deviates slightly during the commutation process, after which the full control recovers; and when the process is complete, FB SMs are able to respond to control system demands. The results confirm the analysis articulated in Section III and simulation results in Section VI.

The advanced features of active/dc power support in dc/ac fault cases are presented in Fig. 23 and 24, respectively.

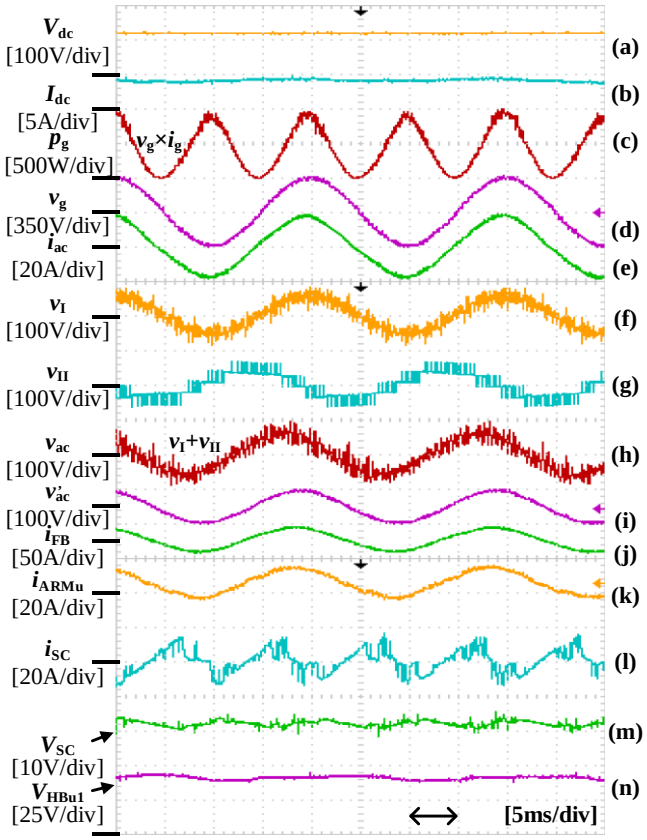

Fig. 21. T-MMC waveforms in an enlarged inductance case.

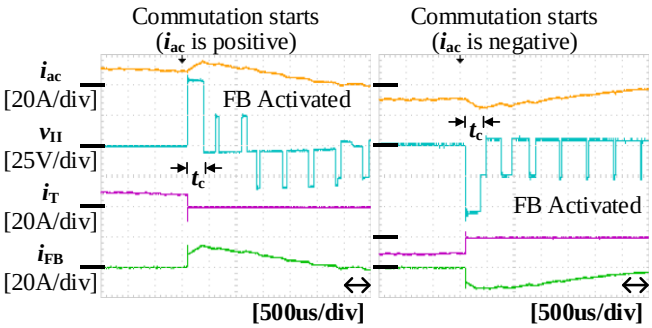

Fig. 22. Stage-II TSG thyristor-commutation process waveforms.

Before the dc fault occurs, the T-MMC operates in the normal mode with Stage-II bypassed by thyristors for higher efficiency, see Fig. 23(e)-(h). The dynamics in Fig. 23(a)-(d) illustrate that ac-side active power injection continues when the dc voltage collapses. In Fig. 23(e)-(h), Stage-II is activated and starts generating ac voltage after the commutation process, whereas Stage-I arms are bypassed with only reactive power consumption. During the dc fault, no dc offset exists within the Stage-I arm current, and the HB SMs are bypassed, with constant capacitor voltages, see Fig. 23(i) and (l). Also, the integrated SCs begin discharging, to provide the required power for the ac side, see Fig. 23(j) and (k).

The T-MMC shifts from the normal mode (Stage-II is bypassed) to a double stage active mode when the ac fault occurs, see Fig. 24(e)-(h). After the successful commutation,

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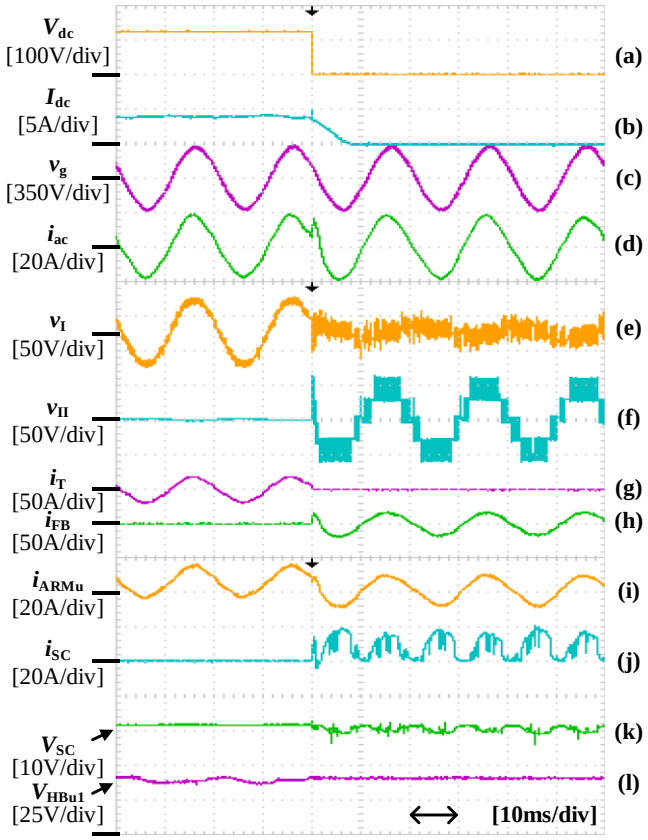

Fig. 23. Waveforms of T-MMC based ESS in the dc fault case.

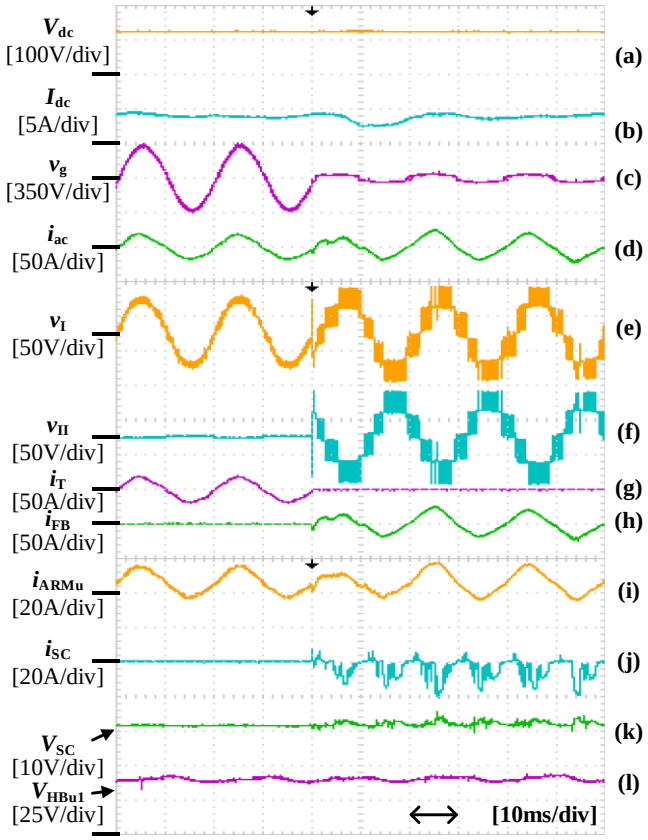

Fig. 24. Waveforms of T-MMC based ESS in the ac fault case.

Stage-II starts to generate ac voltage and compensate the active power from Stage-I. DC power remains after a transient period despite the faulty ac grid, see Fig. 24(a)-(d). Stage-I continues operating, with upper arm current and an SM voltage shown in Fig. 24(i) and (l). Also, the integrated SCs within Stage-II FB SMs charge during the ac fault, absorbing the active power, see Fig. 24(j) and (k).

VIII. Conclusion

A T-type MMC referred to as T-MMC has been proposed in this paper. Flexible operation based on the dual-stage topology can perform ac/dc side protective and supportive functions, such as ac/dc fault isolation, reactive power enlargement, flexible ESS integration, etc. A novel thyristor-SM group for the Stage-II has been presented, with its commutation mechanism and converter-level merits elaborated. As a result, both high efficiency and dc-fault tolerance are achieved by the T-MMC, which was highlighted by comparing with other typical MMCs. The effectiveness of the proposed T-MMC was demonstrated through simulation and experimentation. With the articulated advantages, the T-MMC can be used in robust ac/dc power systems and critical motor drive applications.

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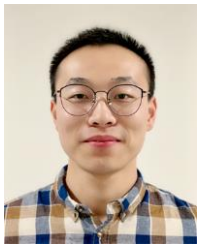

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